

1756

PATENT

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Date: 9/29/03

John M. Ling  
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of:

Applicant(s): Khoi A. Phan, *et al.*

Examiner: John S. Ruggles

Serial No: 10/050,417

Art Unit: 1756

Filing Date: January 16, 2002

Title: METHODS AND SYSTEMS FOR CONTROLLING RESIST RESIDUE  
DEFECTS AT GATE LAYER IN A SEMICONDUCTOR DEVICE  
MANUFACTURING PROCESS

Mail Stop Non-Fee Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

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**REPLY TO OFFICE ACTION DATED JUNE 27, 2003**

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Dear Sir:

Favorable reconsideration of the above-identified patent application is respectfully requested in view of the amendments and comments below.

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